PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-017941
(43)Date of publication of application : 19.01.1996

(51)Int.Cl. H01L 21/8242
H01L 27/108
H01L 27/04
H01L 21/822
H01L 21/8238
H01L 27/092

(21)Application number : 06-169050
(22)Date of filing : 28.06.1994

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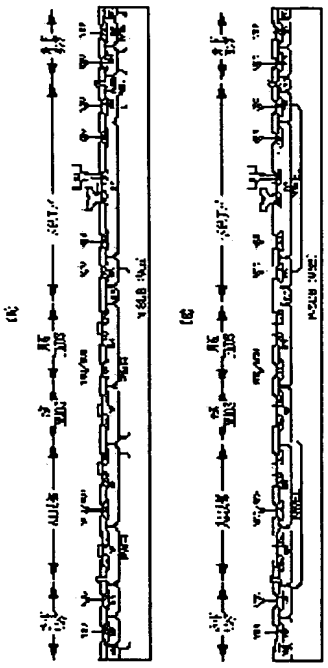
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PURPOSE: To increase the storage capacity of a memory array and improve the refresh characteristics, by supplying only the necessary and minimized back bias voltage to a P-type well where a memory array part is formed, and forming a specified I/O circuit.
CONSTITUTION: A memory array part and an I/O circuit are formed. The memory array part is constituted by arranging dynamic memory cells in a matrix. A P-type well region BP where the memory array is formed is formed in an N substrate N-SUB, and a substrate bias voltage VBB like-IV is supplied. That is, a back bias voltage of a small absolute value which is optimum to refresh characteristics is supplied. A back bias voltage wherein the under shoot voltage is considered and the absolute value is increased is supplied to the P-type well region BP where an N channel MOSFET constituting an I/O part is formed. Thereby a leak current is reduced, refresh characteristics are improved, and under shoot countermeasure is obtained.



LEGAL STATUS

[Date of request for examination] 22.08.2000
[Date of sending the examiner's decision of rejection] 17.02.2004
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]